REMARKS/ARGUMENTS

In the Office Action mailed December 22, 2009, claims 1 and 3-24 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Claim Rejections under 35 U.S.C. 103

Claims 1 and 3-24 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Churchill et al. (U.S. Pat. No. 6,115,836, hereinafter Churchill)
Irrinki et al. (U.S. Pat. No. 5,822,228, hereinafter Irrinki)
Savir (U.S. Pat. No. 5,642,362, hereinafter Savir)
Choi (U.S. Pat. No. 6,342,115, hereinafter Choi)

In particular, claims 1, 3-13 and 16-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill in view of Irrinki and Savir. (For clarification, the Office Action states that claim 2 is also canceled based on the same combination of cited references, but claim 2 was canceled.) Claims 14, 15, and 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill and Irrinki, in view of Choi. However, Applicants respectfully submit that these claims are patentable over Churchill, Irrinki, Savir, and Choi for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Churchill, Irrinki, and Savir because the combination of cited references does not teach all of the limitations of the claim. Claim 1 recites:

A method comprising:
receiving an internal clock signal from a clock monitor of the self-timed memory;

receiving an external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;

receiving a control signal;

providing, in dependence upon the control signal, the internal clock signal to at least one internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal to the at least one internal memory block during a test mode of the self-timed memory, wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern; and

detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test-mode of the self-timed memory.

(Emphasis added.)

In contrast, the combination of Churchill, Irrinki, and Savir does not teach all of the limitations of the claim. For reference, the Office Action relies on Churchill as purportedly teaching the limitations which relate to providing the external clock signal to different internal memory blocks according to a predetermined test pattern. However, Churchill does not teach the indicated limitation because none of the cited portions of Churchill describes a predetermined test pattern.

1. The Examiner's stated understanding of the claim language is imprecise and improper and does not establish the scope of the claim.

As a preliminary matter before addressing the specific teachings of the cited references, it will be useful to discuss the Examiner's treatment of the claim language. In the Office Action, the Examiner states:

> Examiner understands the amended limitation of a predetermined test pattern to be equivalent to control signals used to enable and disable clock distribution (specification, page 6, lines 22 – 24).
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> Office Action, 12/22/09, page 3.

Despite the Examiner's stated understanding of the claim language, it should be noted that the scope of the claims is determined by the language of the claims and not by the paraphrased statements of the Examiner. Moreover, in this instance, the Examiner's

statements are imprecise because the Examiner attempts to generalize the language of the claim to a point that disregards specific language recited in the claim. For example, the Examiner's stated understanding of the claim language disregards the recited language of a predetermined test pattern and, instead, merely asserts that the language refer distribution, generally. However, this generalization of the claim language is imprecise and should not be used to determine the scope of the claim or the extent of the prior art teachings that would be necessary to show anticipation or obviousness of the precise claim language.

Additionally, it should be noted that the Examiner's stated understanding of the claim language is further improper because the Examiner relies on the specification of the present application in order to determine equivalence of limitations of the claim. The MPEP specifically prohibits this approach within a rejection under 35 U.S.C. 103, stating:

> In order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency must be recognized in the prior art, and cannot be based on applicant's disclosure or the mere fact that the components at issue are functional or mechanical equivalents. In re Ruff, 256 F.2d 590, 118 USPQ 340 (CCPA 1958).
> MPEP 2144.06 (emphasis added).

Thus, the Examiner's reliance on the specification of the present application in order to establish equivalence of the limitations of the claim is improper because equivalence cannot be based on Applicants' disclosure.

In light of the facts that the Examiner's statement is imprecise and disregards specific limitations recited in the claim, and also is improper, Applicants submit that the Examiner's stated understanding of the indicated limitations cannot be used to determine the scope of the claims. Rather, the scope of the claims is established by the specific language recited in each claim.

Additionally, the Examiner's stated understanding cannot be used to distort the scope of the claims for the purpose of showing obviousness under 35 U.S.C. 103 based on the cited references. Therefore, the Examiner's statements which address the teachings of the cited references relative to the Examiner's stated understanding are

inapposite and unrelated to the actual language of the claims, and furthermore are insufficient to establish a *prima facie* case of obviousness for the corresponding rejections presented in the Office Action.

2. The cited portion of Churchill, at column 19, lines 5-10, does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern.

The assertion that the subject matter described in Churchill at col. 19, lines 5-10, purportedly teaches the indicated limitations of the claim is incorrect and is not supported by the actual disclosure of Churchill. For reference, this cited portion of Churchill is reproduced herein:

> Thus, the function of the burn-in test may be enhanced when bit 5 is enabled, thereby allowing an external clock signal to replace an internal clock signal when the external clock signal has a larger pulse width than that generated internally by clock pulse generator 900.
> Churchill, col. 19, lines 5-10 (emphasis added).

As explained in Applicants' previous response, these teachings do not relate to or teach providing an external clock signal to different internal memory blocks according to a predetermined test pattern. Although the description referenced in column 19 refers to an external clock signal, the indicated description nevertheless is insufficient to teach any conditions related to a predetermined test pattern used to provide the external clock signal to different internal memory blocks. More specifically, although the general description which includes the cited portions of Churchill relates to using an external clock signal which has a larger pulse width than that generated internally by a clock pulse generator, this description is insufficient to teach providing an external clock signal to different internal memory blocks according to a predetermined pattern. Therefore, the cited portion of Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim.

For the reasons presented above, the combination of Churchill, Irrinki, and Savir does not teach all of the limitations of the claim at least because the cited portion of Churchill does not teach providing an external clock signal to different internal memory

blocks according to a predetermined pattern, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Churchill, Irrinki, and Savir because the combination of cited references does not teach all of the limitations of the claim.

3. The cited portion of Churchill, at column 4, lines 49-67, does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern.

The assertion that the subject matter described in Churchill at col. 4, lines 49-67, purportedly teaches the indicated limitations of the claim is incorrect and is not supported by the actual disclosure of Churchill. For reference, this cited portion of Churchill is reproduced herein:

> Programmable scan interface 212 provides a mechanism for programmably altering various signals within SRAM 200 to improve the observability and characterization of circuitry within SRAM 200. For example, programmable scan interface 212 may output from one to n control signal(s) on line(s) 224. Control line(s) 224 may comprise from one to n lines (or from one to n/m lines, where m is the value of an m-to-1 multiplexer coupling the control signals from programmable scan interface 212 to control line(s) 224) or busses. One of the control signals may configure output register 218 to become transparent; that is, output register 218 may switch from synchronous to asynchronous operation, such that data may be passed directly through output register 218. This may increase the ability to monitor and test the operation of the memory core without interference and/or masking effects caused by output register 218. One or more of the control signals may also be coupled to input register 216 to configure input register 216 to become transparent.
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> Churchill, col. 4, lines 49-67.

These teachings of Churchill also fail to teach providing an external clock signal to different internal memory blocks according to a predetermined test pattern. Although the description referenced in column 4 programmably altering various signals, the general reference to "various signals" is insufficient to teach the specific limitations of a predetermined test pattern used to provide the external clock signal to different internal memory blocks. Moreover, the specific examples of using control signals to configure input or output registers to become transparent are also insufficient to teach the specific

indicated limitations of the claim. Therefore, the cited portion of Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim.

For the reasons presented above, the combination of Churchill, Irrinki, and Savir does not teach all of the limitations of the claim at least because the cited portion of Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Churchill, Irrinki, and Savir because the combination of cited references does not teach all of the limitations of the claim.

4. The cited portion of Churchill, at column 5, lines 13-25, does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern.

The assertion that the subject matter described in Churchill at col. 5, lines 13-25, purportedly teaches the indicated limitations of the claim is incorrect and is not supported by the actual disclosure of Churchill. For reference, this cited portion of Churchill is reproduced herein:

> Programmable scan interface 212 may also programmably alter the clock pulse width of CCPULSE on line 222. Programmable scan interface 212 may accomplish this by outputting one or more control signals on line 226, which may comprise one or more control lines as described above for control line(s) 224. Additionally, programmable scan interface 212 may replace CCPULSE on line 222 with an external periodic signal (e.g., a timing signal or the CLK signal) having a characteristic frequency (preferably lower than the corresponding frequency of one of the internal clock signals) by activating one or more control signals on line 228. Line 228 may comprise one or more control lines as for control lines 224 and/or 226.
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> Churchill, col. 5, lines 13-25.

These teachings of Churchill also fail to teach providing an external clock signal to different internal memory blocks according to a predetermined test pattern. Although the description referenced in column 5 refers to altering a clock pulse width, the indicated

description nevertheless is insufficient to teach any conditions related to a predetermined test pattern used to provide the external clock signal to different internal memory blocks. Similarly, the description in Churchill of replacing the internal clock signal CCPULSE with an external periodic signal also fails to provide sufficient description to teach a predetermined test pattern used to provide the external clock signal to different internal memory blocks. Therefore, the cited portion of Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim.

For the reasons presented above, the combination of Churchill, Irrinki, and Savir does not teach all of the limitations of the claim at least because the cited portion of Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Churchill, Irrinki, and Savir because the combination of cited references does not teach all of the limitations of the claim.

Independent Claims 9 and 17

Applicants respectfully assert independent claims 9 and 17 are patentable over the proposed combination of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of these claims recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of these claims should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejections of these claims.

Dependent Claims

Claims 2-8, 10-16, and 18-24 depend from and incorporate all of the limitations of the corresponding independent claims 1, 9, and 17. Applicants respectfully assert claims 2-8, 10-16, and 18-24 are allowable based on allowable base claims.

Additionally, each of claims 2-8, 10-16, and 18-24 may be allowable for further reasons, as described below.

The rejections of claims 14, 15, and 21-24 are improper because the Office Action does not establish a *prima facie* case of obviousness for the rejections of these claims. In order to establish a *prima facie* case of obviousness for a rejection of a claim under 35 U.S.C. 103, the Office Action must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

Here, the Office Action fails to provide a rational underpinning to support the legal conclusion of obviousness because the proposed combination of Churchill, Irrinki, and Choi does not address all of the limitations of the claim. Although the indicated rejections rely on the combination of Churchill and Irrinki as purportedly teaching the limitations of the corresponding parent claims (i.e., claims 9 and 20), the reasoning presented in the rejections of the corresponding parent claims recognizes that the combination of Churchill and Irrinki does not teach all of the limitations of the parent claims. Specifically, the reasoning presented in the rejections of claims 9 and 20 acknowledge that Churchill does not teach detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory. Office Action, 12/22/09, page 9 (for claim 9) and page 12 (for claim 20). Additionally, the reasoning in the Office Action does not rely on Irrinki as teaching this missing limitation of Churchill. Rather, the reasoning in the Office Action relies on Savir as purportedly teaching the indicated limitation. However, the reasoning presented in support of the rejections of dependent claims 14, 15, and 21-24 does not rely on Savir in combination with the other references. Thus, there are no references relied on in the stated rejections of claims 14, 15, and 21-24 as teaching detecting a slow-to-rise delay or a slow-to-fall delay, as recited in the corresponding parent claims 9 and 20.

Therefore, there is not a rational underpinning to support the legal conclusion of obviousness because the assertions in the Office Action in support of the rejections of claims 14, 15, and 21-24 do not address all of the limitations of the claims. Consequently, the Office Action fails to establish a *prima facie* rejection for claims 14, 15, and 21-24 because the Office Action does not assert or show how the proposed combination of Churchill, Irrinki, and Choi might teach detecting a slow-to-rise delay or a slow-to-fall delay, as recited in the claims through incorporation of the limitations from the corresponding parent claims 9 and 20. Accordingly, Applicants respectfully submit that the rejections of claims 14, 15, and 21-24 under 35 U.S.C. 103(a) should be withdrawn because the Office Action fails to establish a *prima facie* case of obviousness in support of the stated rejections.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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